

ABSTRACT

A semiconductor structure and method for chip dicing. The method comprises the steps of (a) providing a semiconductor substrate; (b) forming first and second device regions of first and second chips, respectively, in and at top of the semiconductor substrate, wherein the first and second chips are separated by a semiconductor border region of the semiconductor substrate; (c) forming N interconnect layers directly above the semiconductor border region and the first and second device regions, wherein N is a positive integer, wherein each layer of the N interconnect layers comprises an etchable portion directly above the semiconductor border region, and wherein the etchable portions of the N interconnect layers form a continuous etchable block; (d) removing the continuous etchable block by etching; and (e) cutting with a laser through the semiconductor border region via an empty space of the removed continuous etchable block to separate the first and second chips.